Comparative Analysis of Universal Shift Register with and without Clock Gating in VLSI Design

Y. Sowmya[0009-0008-7011-3509], K. Suganthi[0000-0002-0374-4190]

and Vijayakumar Ponnusamy[0000-0002-3929-8495]

Department of ECE, College of Engineering & Technology, SRM Institute of Science and Technology, Kattankulathur, Chengalpattu -India-603203

sy8190@srmist.edu.in, suganthk@srmist.edu.in, vijayakp@srmist.edu.in

Abstract.
One essential component of contemporary VLSI circuit design is effective power management. A popular method for reducing dynamic power usage is clock gating, which selectively disables the clock signal to registers that are not in use. In this study, two variants of a 4-bit Universal Shift Register (USR) written in Verilog HDL - one with and one without clock gating - are compared in detail. Using a 32nm CMOS technology library and Synopsys Design Compiler, the design is synthesized and examined to determine how it affects important performance parameters including area, power consumption, gate count, and timing. The results show that clock gating substantially minimizes extravagant clock switching and dynamic power dissipation while introducing additional logic overhead, resulting in increased area and gate count. Clock gating improves power efficiency, but implementing it into practice might present problems like complex synthesis limitations, propagation delays, and glitches. For the purpose of evaluating these trade-offs across a variety of design factors, a thorough comparative analysis is carried out. a 4-bit Universal Shift Register (USR) with and without clock gating is compared using a 32nm CMOS technology. Clock gating reduces sequential power by 4.05% while increasing area by 16.54% (67.12 µm² to 78.22 µm²) and leaky power by 27.38%. It enhances timing with a 6.67% decrease in critical path delay (0.30 ns to 0.28 ns), even if the overall dynamic power increases by 6.78%. These findings demonstrate the trade-offs of clock gating, which makes it an essential method for designing VLSIs with low power consumption. The findings shed light on the practicality of clock gating in sequential circuits, most significantly for shift registers, and serve as a framework for designers looking to optimize low-power VLSI designs while balancing power, area, and performance requirements.

Keywords: Clock Gating, Universal Shift Register, Low-Power VLSI, Verilog, Synopsys.

1 Introduction

Power optimization is a critical challenge in VLSI circuit design. Power consumption has grown to be a significant concern due to the increasing transistor density and the need for high-speed computation. A popular method for lowering dynamic power is clock gating, which selectively disables the clock signal [1]. Lower power dissipation results from minimizing needless switching activity by stopping the clock signal to

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dormant registers. However, this results in higher area overhead and design complexity. By developing and evaluating the design using Synopsys tools, this study examines how clock gating affects a 4-bit Universal Shift Register (USR) and assesses power savings, area overhead, and timing performance.

Power dissipation in contemporary VLSI systems is divided into two groups: dynamic power and static power. Transistor leakage currents produce static power, whereas capacitive load charging and discharging during switching events produces dynamic power [2]. Since dynamic power predominates in synchronous circuits, clock gating is a practical way to cut down on needless switching activity. In complicated digital circuits, clock distribution networks have been found to account for approximately 30-40% of overall power usage [3]. Implementing clock gating can dramatically reduce power consumption by guaranteeing that only active components receive the clock signal.

Techniques for clock gating can be broadly divided into three categories: combinational logic-based, latch-based, and flip-flop-based. Flip-flop-based methods are favoured for reliable timing control, while latch-based clock gating is frequently employed in ASIC design because of its minimal power overhead [4]. Functional issues could result from incorrect clock gating implementation, which could generate timing hazards including glitches and undesired clock pulses. 00Therefore, to guarantee proper operation, thorough synthesis and verification are needed.

A 4-bit Universal Shift Register (USR) constructed with and without clock gating is compared in this research to better understand the effects of clock gating in practical applications. Synopsys Design Compiler is used to synthesize the designs, which are then assessed according to timing performance, gate count, area, and power consumption. By offering important insights into the trade-offs between hardware overhead and power efficiency, the findings support the ongoing attempts to optimize sequential circuits for low-power VLSI design.

2 Related work

A number of research have looked into register designs that use less power. The usefulness of clock gating in lowering power consumption was covered by the authors in [2]. Comparing different clock gating strategies, another study [3] revealed notable power reductions at the expense of greater complexity. Timing and area trade-offs in clock-gated circuits were examined in research in [4][5]. Clock gating has been shown to dramatically lower power consumption, but if done incorrectly, it can cause glitches and longer propagation delays. Furthermore, in order to specifically maximize power savings in various circuit components, fine-grained clock gating techniques have been developed in [6]. By offering a thorough synthesis and implementation study of clock-gated USRs, this work builds on earlier research.

3 Methodology

The Universal Shift Register (USR) is written in Verilog HDL and includes multiplexers and D flip-flops. It is capable of four operations: parallel load, shift left, shift right, and hold state. There are two variants of the design in use:

3.1 Universal Shift Register Without Clock Gating:

A traditional design in which the clock signal is always present, independent of the register's mode of operation. Even in the absence of a shifting operation, every clock cycle in this system activates every flip-flop. As a result of the redundant switching activity, unneeded power is consumed. Its structure is simpler, though, and it does not require the extra logic cost that comes with clock gating. Although continuous clocking guarantees that timing is not significantly affected, large-scale circuits may experience increased dynamic power dissipation. This design is frequently utilized in low-power or smaller circuits where extra gating logic may not be required, despite its shortcomings.

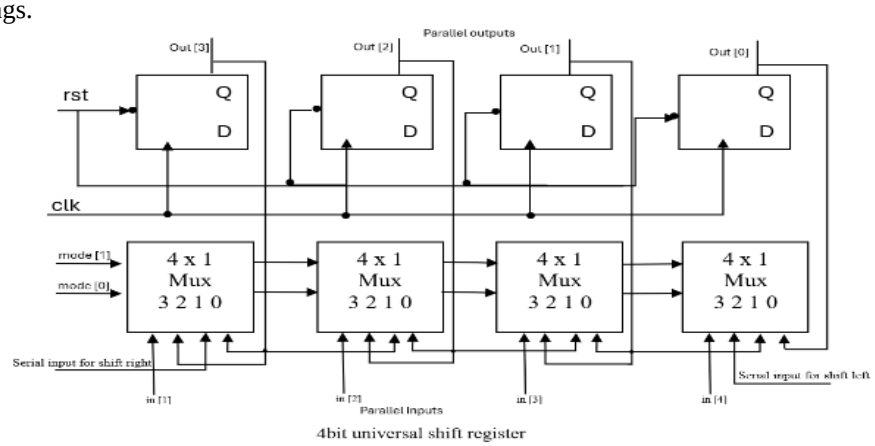

Fig. 1. Universal Shift Register without Clock Gating

3.2 Universal Shift Register With Clock Gating

Implements an enable-based clock gating method to disable clock pulses when no state transition occurs, lowering dynamic power usage. This design adds a second clock gating circuit that, depending on the enable signal, selectively permits the clock signal to propagate. The gated clock stays dormant in the absence of a data transition, reducing power consumption and avoiding needless register switching. In sequential circuits, this technique dramatically lowers dynamic power, particularly in systems with idle clock cycles. But putting clock gating into practice adds more logic, which increases the space and number of gates. Additionally, caution needs to be used to guarantee correct time synchronization and steer clear of any issues that can compromise data integrity.

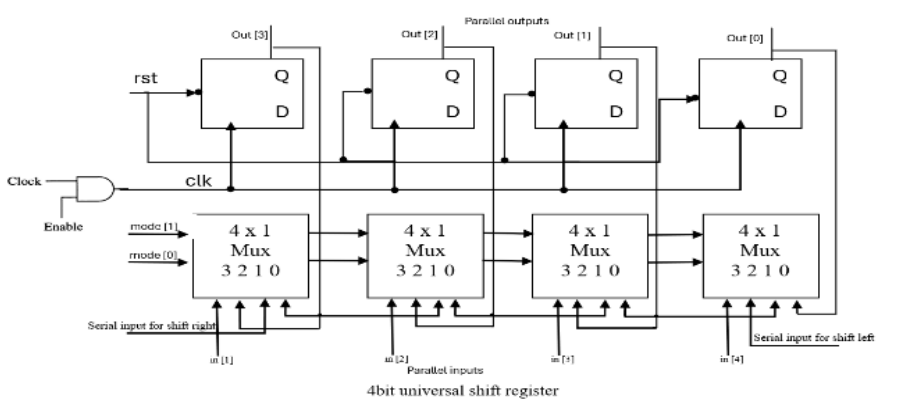

Fig. 2. Universal Shift Register with Clock Gating

4 Implementation

Clock gating is accomplished by employing an enable signal to control clock distribution to the registers. The gated clock stays low when no shift operation is needed, avoiding needless toggling of sequential parts. In order to prevent excessive logic overhead that could negate power savings, the implementation is carefully designed. The Verilog specifications for both USR versions are generated using Synopsys Design Compiler with a 32nm standard-cell library [5]. To maximize performance and space utilization, the physical design approach incorporates clock tree synthesis (CTS), power routing, and floor planning [6].

5 Experimental setup

A well-defined design flow, industry-standard EDA tools, and a systematic evaluation procedure for analysing important design parameters are all part of the experimental setup.

Tools Used: Synopsys Design Compiler is used for logic synthesis throughout the design phase, while Verdi is used for waveform analysis and debugging. These technologies make it possible to evaluate circuit performance effectively and give designers the ability to adjust circumstances for the best outputs.

1. Technology Node: To reflect current VLSI process technology, a 32nm CMOS standard-cell library is used. The technology node is an essential component of the design's power and area characteristics since it affects elements like transistor density, leakage currents, and switching power.
2. Analysis Metrics: The synthesized designs are evaluated using four main parameters:

   Area: The entire hardware footprint, measured in square micrometre's (μm^2). Better integration efficiency is indicated by a decreased area; however, time and power may be impacted.

Power consumption: comprises leakage power (static power dissipation) and dynamic power (switching power resulting from capacitive loads).
Gate Count: Indicates how many logic gates are needed in total for implementation. Although a greater gate count increases power and area, complicated functionality may require it.
Timing Performance: Assesses the maximum operating frequency and crucial path latency. Reducing delay while preventing timing violations due to clock gating is the aim.

6 Experimental results

A comprehensive analysis of the Universal Shift Register (USR) with and without clock gating was conducted using Synopsys Design Compiler. Total area, gate count, dynamic power consumption, and critical path delay are among the evaluation parameters.

1. Simulation Waveforms:

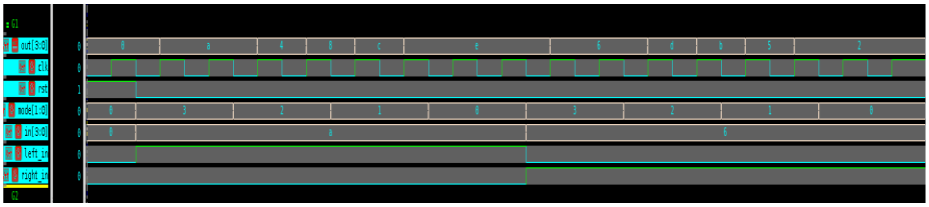

Fig. 3. Simulation waveform of Universal Shift Register Without Clock Gating.

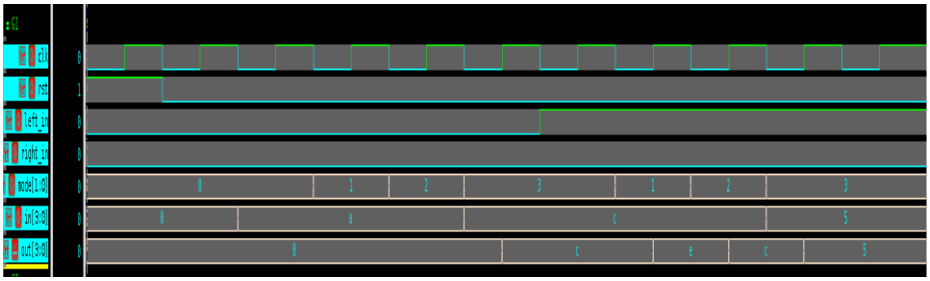

Fig. 4. Simulation waveform of Universal Shift Register With Clock Gating.

The simulation results demonstrate the behavior of the Universal Shift Register (USR) under different conditions. In Fig. 3, the waveform without clock gating shows continuous switching activity, leading to higher power consumption. In contrast, Fig. 4 illustrates the waveform with clock gating, where unnecessary transitions are reduced. This indicates improved power efficiency while maintaining correct functionality. Overall, the use of clock gating effectively minimizes dynamic power without affecting the performance of the system.

2. Schematic Report Analysis:

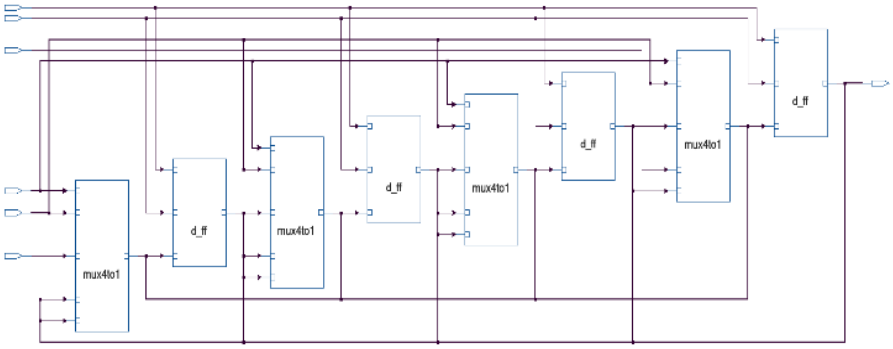

Fig. 5. Schematic of Universal Shift Register Without Clock Gating

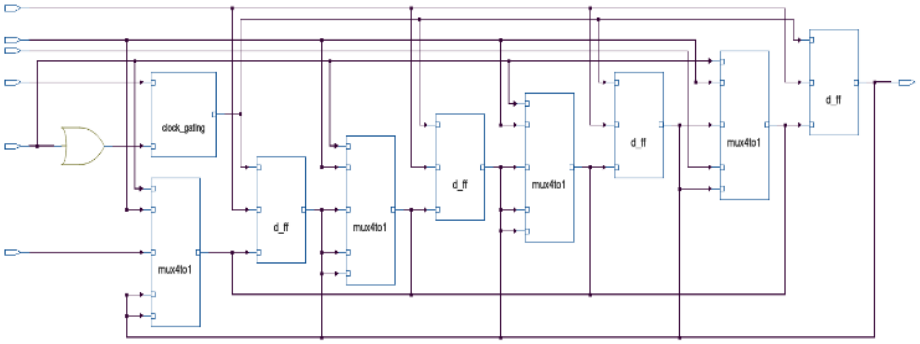

Fig. 6. Schematic of Universal Shift Register With Clock Gating

3. Area Analysis:

The Universal Shift Register (USR) with clock gating exhibits a 16.54% increase in total area (from 67.12 µm² to 78.22 µm²) due to the additional clock gating logic [9]. Sequential cells grow by 25% (from 4 to 5) and combinational cells increase by 23.08% (from 13 to 16) [10] as shown in Table 1. Because of the additional enable logic and clock distribution circuits, the combinational area increases by 14.01% and the non-combinational area by 17.86% [11]. Clock gating is a crucial power optimization approach in VLSI design because, despite its area overhead, it dramatically lowers dynamic power dissipation in large-scale systems [12].

Table 1. Area report Comparison of USR with clock and without clock gating.

Metric	Without Clock Gating	With Clock Gating	Difference	% Increase
Number of nets	27	31	4	14.81%
Number of cells	17	21	4	23.53%
Combinational cells	13	16	3	23.08%
Sequential cells	4	5	1	25.00%
Buf/Inv cells	9	10	1	11.11%
Combinational area	34.55296	39.39232	4.83936	14.01%
Buf/Inv area	11.690624	12.961344	1.27072	10.87%
Non-combinational area	28.464128	33.547009	5.08288	17.86%
Total cell area	62.519424	72.939328	10.4199	16.67%
Total area	67.120199	78.219625	11.0994	16.54%

4. Power Report:

The Universal Shift Register's (USR) power comparison with and without clock gating demonstrates the trade-offs associated with power optimization. Clock gating is a useful method for reducing dynamic power in sequential elements because it reduces needless clock toggling, which results in a 4.05% drop in sequential power usage [10] as shown in Table 2. However, because clock gating requires additional combinational logic, this results in a 6.78% increase in total dynamic power [12].

Table 2: Power report Comparison of USR with clock and without clock gating

Metric	Without Clock Gating	With Clock Gating	Difference	% Change
Cell Internal Power	2.5843 uW	2.6857 uW	+0.1014 uW	+3.92 %
Net Switching Power	1.1577 uW	1.3099 uW	+0.1522 uW	+13.15 %
Total Dynamic Power	3.7419 uW	3.9957 uW	+0.2538 uW	+6.78 %
Cell Leakage Power	96.952 nW	123.504nW	+26.5519 nW	+27.38 %
Sequential Power	1.3674 uW	1.312 uW	-0.0554 uW	-4.05 %
Combinational Power	2.3496 uW	2.6811 uW	+0.3315 uW	+14.11 %

The gating logic adds additional switching activity, as evidenced by the 13.15% increase in net switching power [8]. Additionally, more transistors stay active even while the circuit is idle, increasing leakage power by 27.38% [6]. Although clock gating lowers dynamic power in sequential circuits, the additional gating logic causes a 14.11% increase in combinational power [7]. Overall, clock gating is still advantageous for power-critical applications, particularly in systems with high sequential activity, where

the decrease in needless clock toggling surpasses the combinational power overhead, even with the minor increase in overall power [8].

5. Timing Analysis:

The timing comparison of the Universal Shift Register (USR) with and without clock gating demonstrates a minor difference in data arrival times. The data arrival time is 0.28 ns with clock gating, suggesting a 6.67% reduction in delay, compared to 0.30 ns without it [9].

Table 3: Timing report Comparison of USR with clock and without clock gating.

Metric	Without Clock Gating	With Clock Gating	Difference	% Change
Data Arrival Time	0.30 ns	0.28 ns	-0.02 ns	-6.67%
Clock to Q Delay	0.30 ns	0.27 ns	-0.03 ns	-10%
Output Delay	0.01 ns	0.01 ns	0.00 ns	0%
Timing Constraint	Unconstrained	Unconstrained	-	-

This reduction implies that clock gating improves signal transmission by marginally optimizing the timing path by eliminating pointless transitions in sequential logic [2]. The difference is negligible, though, and how it affects the circuit's total performance is dependent on other limitations like setup and hold times [1]. In real-world applications, more optimization might be necessary to guarantee timing closure because the timing path is unbounded in both scenarios [5]. Clock gating offers enhanced efficiency by marginally lowering the maximum delay while successfully limiting dynamic power consumption in sequential circuits, despite the area and power trade-offs [3].

6. Gate Report:

Significant variations in cell utilization and area consumption are revealed by comparing the designs with and without clock gating at the gate level. The number of cells is increased by 23.5% in the clock gating design, which uses 21 cells, whereas the clock gating design uses only 17 cells [4]. The increased clock gating logic, which includes additional inverters and a latch to operate the gated clock, is the main cause of this increase [2]. The clock-gated design has a 16.7% increase in area, taking up 72.9393 μm^2 as opposed to 62.51942 μm^2 for the non-clock-gated design [6]. The basic architecture of the universal shift register is maintained in spite of this expansion since there are still the same number of flip-flops (dff's) and multiplexers (mux's). With an additional latchx1_rvt utilized to dynamically adjust the clock signal, clock gating mainly impacts the clock distribution logic.

This comparison shown in Table 4 highlights the primary trade-off between area usage and power efficiency. Clock gating adds extra logic, which results in a slight increase in area, but it also drastically lowers dynamic power usage by turning off inactive circuit components [9]. Clock gating should therefore be chosen based on design limitations and optimization objectives, weighing complexity and space overhead against power savings.

Table 4: Gate report Comparison of USR with clock and without clock gating.

Metric	Without Clock Gating	With Clock Gating	Difference	% Change
Total Cells Used	17	21	4	23.50%
Total Area (µm²)	62.51942	72.9393	10.42	16.70%
Flip-Flops (DFFs)	4	4	0	0%
Multiplexers (MUXs)	4	4	0	0%
Inverters (INVX)	9	10	1	11.10%
Latch for Clock Gating	0	1	1	New

7. Physical Design:

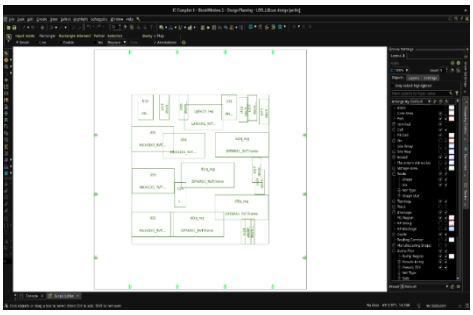

Fig. 7. Floor planning of USR With Clock Gating.

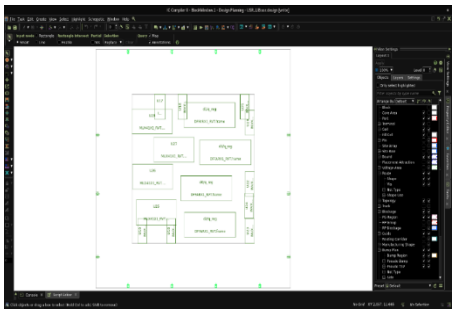

Fig. 8. Floor planning of USR Without Clock Gating.

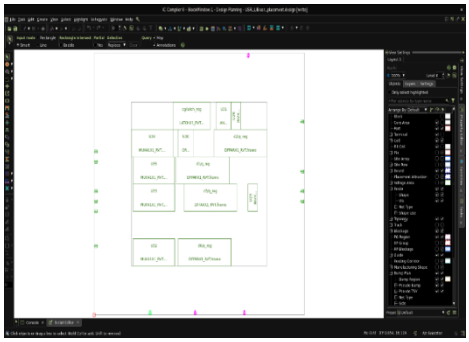

Fig. 9. Placement of USR With Clock Gating

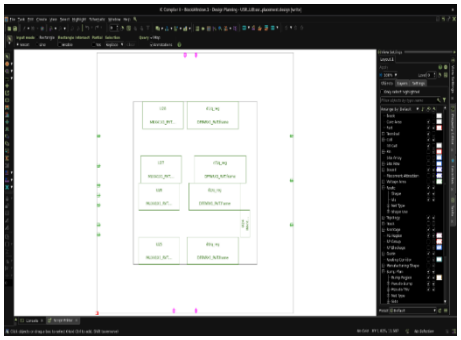

Fig. 10. Placement of USR Without Clock Gating

Power Planning:

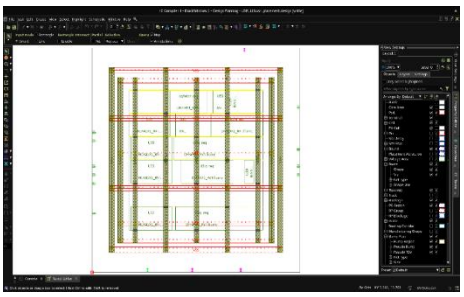

Fig. 11. Power Planning of USR With Clock Gating

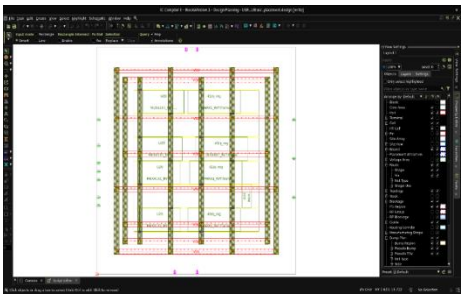

Fig. 12. Power Planning of USR Without Clock Gating

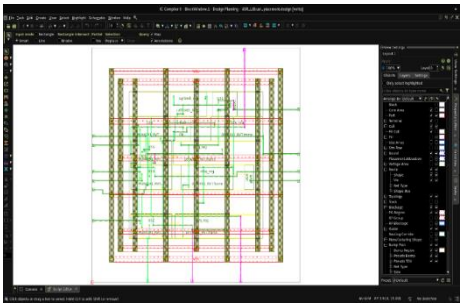

Fig. 13. Routing of USR With Clock Gating

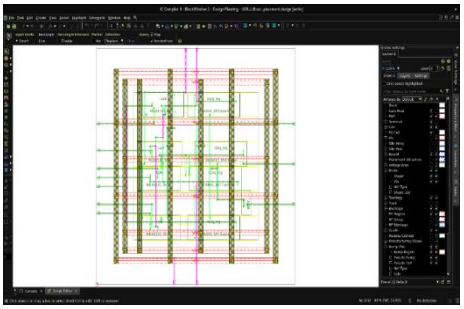

Fig. 14. Routing of USR Without Clock Gating

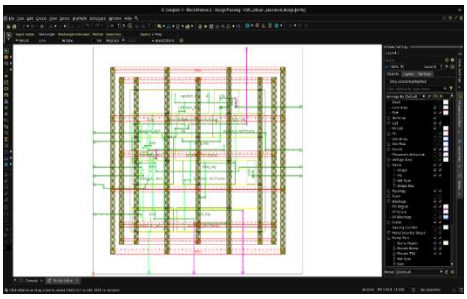

Fig. 15. Clock Tree Synthesis of USR With Clock Gating

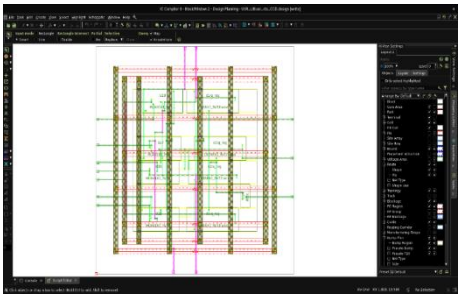

Fig. 16. Clock Tree Synthesis of USR Without Clock Gating

7 Results and discussions

The 4-bit Universal Shift Register (USR) with and without clock gating was evaluated using Synopsys Design Compiler and a 32nm CMOS standard-cell library. Key design parameters like area, power consumption, gate count, and timing performance were the main focus of the investigation. The findings show that clock gating adds an overhead in terms of size and circuit complexity even while it helps with power optimization.

According to the area comparison, the clock-gated design takes up 78.22 μm^2, which is 16.54% more space than the non-gated design's need of 67.12 μm^2. The extra clock gating logic, which includes an enable signal, latch, and additional inverters to regulate the gated clock signal, is responsible for the area increase. In addition, the design's logic cell count rises from 17 to 21, indicating a 23.5% increase in logic complexity. Clock gating becomes extremely advantageous in bigger systems because clock distribution accounts for a significant amount of power consumption, even though this increase could seem enormous for small-scale designs.

The elimination of unnecessary clock toggling in inactive conditions results in a 4.05% reduction in sequential power usage, based on the data. A 6.78% increase in total dynamic power, mostly due to more switching activity in the combinational gating logic, counteracts this advantage. Additionally, even under idle conditions, the additional clock gating elements introduce more active transistors, resulting in a 27.38% increase in leakage power. Clock gating greatly lowers the total clock-related switching power in complex VLSI systems, despite the fact that these effects may result in higher power consumption in tiny circuits.

Data arrival time in the clock-gated design drops from 0.30 ns to 0.28 ns, indicating a 6.67% reduction in critical path delay, according to a timing analysis of the two designs. Optimized clock distribution, which reduces unnecessary sequential state changes, is responsible for this increase. However, improper clock gating implementations can cause glitches and timing violations, requiring careful design considerations that ensure setup and hold time requirements are met.

8 Conclusion

In this study, the size, power, and timing performance of a 4-bit Universal Shift Register (USR) with and without clock gating are compared in depth. The additional clock control circuitry, which includes latches and inverters, is the main reason for the clock-gated design's 16.54% increase in area. The gate count increases by 23.5%, indicating a considerable increase in design complexity.

Clock gating minimizes unnecessary clock transitions in inactive registers by effectively decreasing sequential power by 4.05%. However, it causes a 27.38% increase in leakage power and a 6.78% increase in total dynamic power due to the more applicants switching in combinational logic. Clock gating optimizes clock distribution by eliminating unnecessary toggling in sequential sections, which results in a slight improvement in critical path delay (6.67%), based on the timing analysis.

The advantages of clock gating in power-critical applications exceed its drawbacks, notwithstanding the area overhead. It is an essential technique in modern VLSI design, particularly in large-scale digital circuits, where clock-related power dissipation is significant. To further improve power efficiency while reducing space overhead, future research could investigate machine learning-based optimization techniques, multi-level clock gating structures, and adaptive clock gating methods.

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Disclosure of Interests - The authors declare that there are no conflicts of interest regarding the publication of this paper.

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